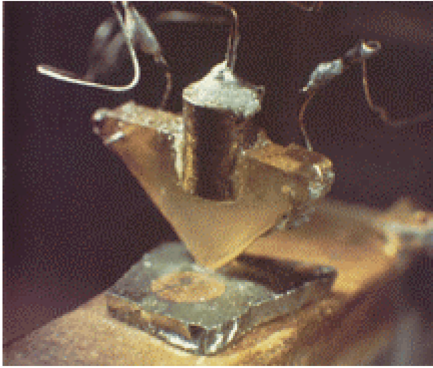
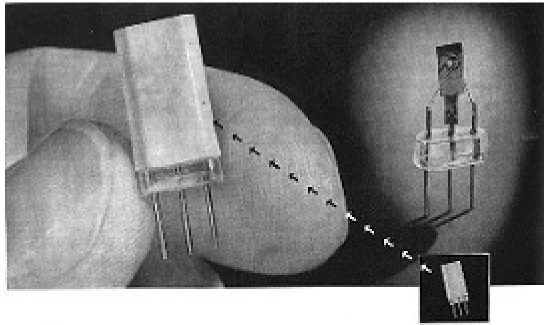
The Chemistry of Semiconductor Integrated Circuit



The Point Contact Transistor

The Story of the Incredible Shrinking Transistor

Chemistry 508
Thesis Presentation
Cristobal Carambo
August 2005



Transistors circa 1960

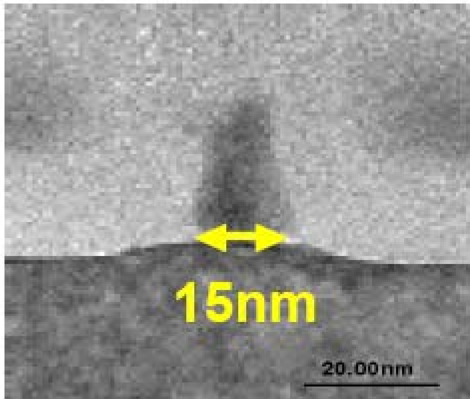
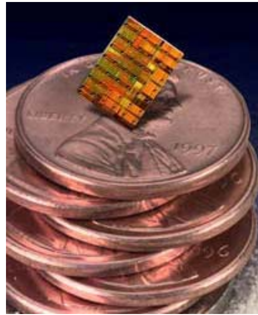


Figure 5: TeraHertz transistor with 15nm gate



IBM CMOS Chip

The great eras in human history are often characterized by the dominant economic technology of the time (The Iron Age, The Stone Age), the nature of social political thought (The Enlightenment, The Renaissance, The Victorian Era), or in terms of shifts in fundamental economic or industrial modes of production (The Agricultural, Scientific, or Industrial Revolutions). It is difficult however, to characterize contemporary human history in such broadly general terms, as modern life is too complex and emergent for any reductive description. Although our global reality defies simple description, the reliance on digital electronic devices is a reality that pervades the daily life of almost every individual on planet earth.

Digital electronics devices have so affected every aspect of our industrial, educational, and personal endeavors that we speak of contemporary history as the time of the Digital Revolution. The revolution's affects are widespread because digital electronic devices are powerful, economical, and readily adapted to countless societal and personal uses. Digital devices are powered by astonishingly small, reliable integrated circuits fabricated on and in the surface of semiconducting substances. The fabrication processes that can place millions of electronic devices on circuits the size of an American penny are largely responsible for the dominance of digital electronics.

Digital devices are especially suited to applications that store, retrieve, and process vast amounts of information. The information industry (corporations that process data, the hardware / software they use, and the technologies that fabricate informational devices) is quickly becoming the dominant industrial activity in postindustrial society. The role of the information technology is so central to modern society that we refer to our time as the Information Age.

> During the past fifty years, the firms that provide our computers, communications technology, and information services, have become a vitally important underpinning to our economy and to our society -- both in terms of their own economic strength, and in terms of their productivity impacts on other industry sectors, from automobile and aircraft manufacturing, to pharmaceutical research, to overnight package delivery services. To an increasing degree, information technology is becoming so embedded in everyday applications that it is becoming nearly invisible (Lasowska, 1997).

Of all electronic devices, the modern computer is recognized as the preeminent device of the information age as it makes access to information via software, local wide area networks, and the Internet a part of every corporate and individual life. The integrated semiconductor circuits that store information (i.e. DRAM, SRAM) and the microprocessors that control logic, mathematical, and system integration (i.e. Intel Pentium 4, Celeron processor) have made it possible to manufacture the small, powerful and (relatively) inexpensive computing systems that have made the Information Age a reality.

The history of the semiconductor integrated circuit is a combination of technological and scientific discoveries in a wide variety of disciplines. Two developments in electronic circuitry (the invention of the point contact and junction transistors, and the development of the semiconductor integrated circuit) are credited as the pivotal events of the past century (Sze, 2002; Riordan & Hoddeson 1997). The

inventions are so important that their inventors have all received Nobel Prizes their work: John Bardeen, Walter Brattain, and William Schockley received the 1956 Nobel in physics for their work on the point contact and junction transistor. Jack Kilby shared the 2000 prize in physics for his creation of the semiconductor integrated circuit.

Prior to invention of the transistor, electronic devices were filled with vacuum tubes that functioned as resistors, diodes and capacitors. The required vacuum, the glass enclosure and the heat generated by the fragile tubes meant that electronic devices were large, inefficient, and costly. (See ENIAC statistics in Appendix A). Bardeen and Brattain's 1947 point- contact transistor (a piece of gold foil, a plastic triangle and a slice of germanium, ~ 0.5 inches long) functioned as a semiconducting amplifier. Ralph Bown of Bell Labs announced the invention:

> We have called it the Transistor because it is a resistor or semiconducting device which can amplify electrical signal as they are transferred through it form input to output terminals." Ralph Bown, June 30, 1948 Press Conference announcing the Transistor (Riordan & Hoddeson 1997, p.164)

William Shockley refined the design of the point contact transistor and created the Junction Transistor in early 1948. The Schockley transistor was a "sandwich" of p and n type germanium. The junction transistor eliminated wires and points of contact. Gordon Teale and Morgan Sparks perfected the junction transistor technology in 1950 by selectively doping areas of a germanium crystal with gallium (p doping) and antimony (n doping). Once doped, contact points were etched into the n regions and contact wires were attached (Riordan & Hoddeson, 1997). The technology of selectively doping and exposing areas on the surface of a semiconducting material remains to this day. By 1957, the transistor production had risen to ~ 30 million per year, the cost of all semiconducting devices (diodes, capacitors, resistors,) plummeted and annual revenues reached of the semiconducting industry grew beyond 100 million. Semiconducting devices displaced vacuum tubes and made new generations of electronic devices possible, however their size (immense by today's standards) and the complexity of wiring larger more intricately connected circuits limited the further growth of the electronics industry (Riordan & Hoddeson, 1997).

The problems posed by the wiring of discrete electronic devices were solved by Jack Kilby's 1959 invention of the semiconductor integrated circuit. Mr. Kilby's invention (patented on February 6,1959 as "Miniaturized Integrated Circuits") was revolutionary because it fashioned all of the components of an integrated circuit (the original circuit was an oscillating circuit) from the semiconductor germanium. "Extreme Miniaturization" and the use of only one substrate material were the stated goals of the invention. The oscillating circuit that Mr. Kilby and Texas Instruments (Mr. Kilby's employer) presented to the public later that year was about the size of a pencil point, however it performed better than circuits many times it's size (Riordan & Hoddeson, 1997).

While Kilby and Texas Instruments were developing their integrated circuit, Robert Noyce and seven other scientists (one of which was Gordon Moore) at Fairchild Semiconducting Corporation were perfecting a similar semiconductor integrated circuit. Mr. Noyce (the head of research) and Gordon Moore (head of production

engineering) would leave in 1968 to establish Intel Corporation. Noyce and Jean Hoerni (a physicist at Fairchild) developed a manufacturing process that began by growing a layer of silicon dioxide onto the surface of crystalline silicon (planar manufacturing). Photolithography was used to imprint the desired pattern onto the silicon. Once patterned, the selected areas were exposed using a chemical etchant. These areas were selectively doped, and then re oxidized. Fairchild's use of an oxide layer as an insulator between sectors of the devices effectively ended the use of germanium in semiconducting electronic devices because germanium has no naturally occurring oxide. Noyce also perfected the method of layering metal through openings in the SiO_2 insulation to interconnect all of the devices at one time. These modifications made it possible to fabricate large numbers of transistors and other electronic devices upon a silicon substrate at the same time. The Noyce planar manufacturing process was patented in 1959 as a means to

> "provide improved device and lead structures for making electrical connections to the various semiconductor regions, and make unitary circuit structures more compact and more easily fabricated in small sizes" (Riordan & Hoddeson p. 265)

The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) is the most important device in modern integrated "circuits such as memories and microprocessors because of its low fabrication cost, small size, and low power consumption" (Shimura, 106). They are ideally suited to the logic requirements of digital electronics as they can be easily programmed to be on (logic state =1) or off (logic state=0). There are currently 200 plus quadrillion transistors in use today. Table 1 shows the effect that transistor density has on the speed of operations; Millions of Instructions Per Sec., data flow, and feature size).

Table 1

Name	Date	Transistors	Microns	Clock speed	Data width	MIPS
8080	1974	6,000	6	2 MHz	8 bits	0.64
8088	1979	29,000	3	5 MHz	16 bits 8-bit bus	0.33
80286	1982	134,000	1.5	6 MHz	16 bits	1
80386	1985	275,000	1.5	16 MHz	32 bits	5
80486	1989	1,200,000	1	25 MHz	32 bits	20
Pentium	1993	3,100,000	0.8	60 MHz	32 bits 64-bit bus	100
Pentium II	1997	7,500,000	0.35	233 MHz	32 bits 64-bit bus	~300
Pentium III	1999	9,500,000	0.25	450 MHz	32 bits 64-bit bus	~510
Pentium 4	2000	42,000,000	0.18	1.5 GHz	32 bits 64-bit bus	~1,700
Pentium 4 "Prescott"	2004	125,000,000	0.09	3.6 GHz	32 bits 64-bit bus	~7,000

Semiconductor

Semiconductors are elements or combination of elements whose resistivity (ρ) and hence conductance is between that of conductors and insulators. The resistivity of conductors is between ~10^{-8} and 10^{-12} Ω cm: insulators ~10^{9} and 10^{19} Ω cm, while that of semiconductors varies between 10^{-5} and 10^{2} Ω cm (silicon has a resistivity between 0.1 and 60 Ωcm) (Giancoli, 2002). Semiconductors are intermediate between insulators and conductors because their band gap (the energy difference between the highest level of their valence band and the lowest level of their conductance band) is relatively small. Molecular orbital theory states that as atoms bond, each type of atomic orbital forms a bonding and non-bonding molecular orbital. Thus whenever n atoms bond, n bonding and n non-bonding molecular orbitals are formed. The Band theory of solids, suggests that as these large numbers of atoms come together (as in a lattice structure), the discrete energy levels of the two types of molecular orbitals merge together to form bands. In solids, the highest occupied energy levels are referred to as the valence band (highest occupied molecular orbitals), while the conduction band (is the lowest unoccupied molecular orbitals (Miesler, 1999). (** The conduction band should technically be referred to as the antibonding band, but for continuity with most textbooks, I will continue to refer to it as the conduction band.) The difference in energy between the two bands is referred to as the band gap, and the energy required for an electron to move between the two bands is referred to as the band gap energy. The conductive properties of insulators, conductors, and semiconductors can be understood from the difference in their band gaps.

Table 3 compares the band gaps and band gap energies of conductors, insulators and semiconductors.

Table 3 Band Gap Energy

Material	Band Gap eV	Band Gap Joules	Population in Conduction Band (300K)
Carbon	5.5	8.8 E –19 Joules	5.11E-19
Silicon	1.11	1.76 E –19 Joules	206,723
Germanium	0.66	1.0 E –19 Joules	1.9E13
α Tin	0.11	1.76 E –20 Joules	8.54 e21

http://www.owlnet.rice.edu/~chem152/lecture/Reading/semibands.html

The Boltzman distribution function can be used to predict the distribution of a given population of particles as a function of temperature and the energy difference between given excited states. The equation $N_i = N_o e^{\frac{-\Delta E}{kT}}$; where N_i is the fractional distribution of a given population N_O, at temperature T, ΔE is the energy difference between given energy levels (the band gap in metals), and k is the Boltzman constant (1.38 E-23 J/K). For given substances one can see that insulators (such as carbon) have virtually no electrons in the conduction band, conductors (tin) have many electrons available for conduction. The number of available electrons for semiconductors (silicon, germanium) is between conductors and insulators and varies based on their respective band gap energies.

Semiconductors are well suited for semiconductor electronics because their resistivity can be altered by the addition of impurities either pentavalent or trivalent atoms to their lattice. The process of adding impurities to an intrinsic (pure) semiconductor (silicon or germanium) is referred to as doping (the impurities are called dopants). Table 2 (Appendix B) shows that the resistivity of silicon varies between 10^{-3} Ω cm to approximately 10^{3} Ω cm for given concentrations of boron or phosphorous.

Figures 1 and 2 illustrates how dopants affect the resistivity / conductance of a semiconductor. In figure 1, the dopant has created a hole as it is missing one of four electrons required to bond with the tetravalent silicon. The hole is a positive charge carrier as it is the site of electron depletion. The addition of phosphorous contributes an extra electron (charge carriers) to the lattice. Silicon is thus ideally suited for integrated circuits as it is quite easy to create areas of differential electrical properties.

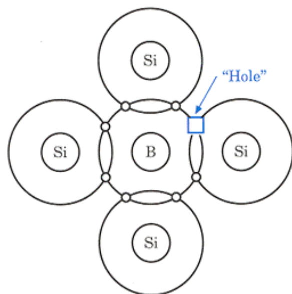


Fig.1

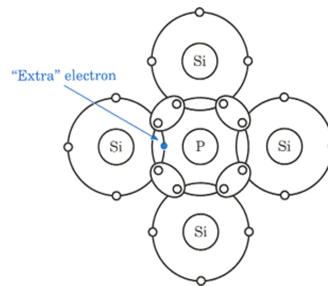


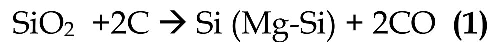
Fig.2

"In terms of percentage, it takes only from 0.000001 to 0.1% of a dopant to bring a semiconductor material to useful resistivity range. This property of semiconductors allows for the creation of regions of very precise resistivity values in the material".
(Van Zant, 1990 p.28)

Preparation of silicon:

The silicon used in the manufacture of microprocessor integrated circuits needs to be of extremely high purity. The required purity is termed the eleven nines: (99.9999999% pure). Given that the concentration of group 3 or group 5 atoms is used to affect electrical character, of the silicon, it is imperative that initial impurities from group 3 elements be no more than 0.3ppba, those from group 5 should be no greater than 1.5ppba and those from metallic ions less than 0.01ppba (Van Zant, 1990). Supply of silicon is abundant as silica (SiO_2) and silicates (quartz, sand, and feldspar) make up ~27.5% of the earth's crust. Silicates as starting materials are reduced with carbon (coke, wood ashes, or coal) at reaction temperatures of about 1500 – 2000°C in arc furnaces. This carbothermic reduction (1) produces silicon which is ~ 98 – 99 % pure.

Trace impurities of Aluminum, Boron, Iron, phosphorous carbon and zinc make up the remaining ~ 1% of MG-Si.



$$SiO_2 + 2C \rightarrow Si\ (Mg\text{-}Si) + 2CO \quad \mathbf{(1)}$$

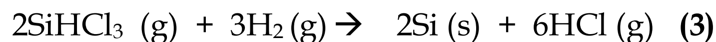
This metallurgical grade silicon (Mg-Si) is powdered and reacted with anhydrous Hydrogen Chloride in a fluidize bed reactor at 300°C **(2).** The reaction of silicon with HCl produces silane and the chlorosilanes: SiH_4, $SiCl_4$, $SiHCl_3$, SiH_2Cl_2, and $SiHCl_3$**.** Of these products, trichlorosilane is the preferred starting material for Semiconductor Grade SG–Si. The following physical properties explain why trichlorosilane is the preferred intermediate:

- It forms at relatively low temperatures: (200 – 400°C)
- Purification is easily accomplished as it is a liquid at room temperature
- It is easily stored, handled and transported
- It will depose on heated silicon (the final purification step) and it reacts quicker and a lower temperature than the other by products

(Shimura 1989 p.117)

$$Si + 3HCl \rightarrow SiHCl_3 + H_2 \quad \mathbf{(2)}$$

Iron, aluminum and boron impurities present in the MG-Si are converted to their halides: $FeCl_3$, $AlCl_3$ and BCl_3. These byproducts are removed by fractional distillation. The concentration of impurities at the end of distillation is 1ppba. (Shimura, 1989, p.117) The purified tricholorsilane is vaporized, mixed with very pure hydrogen gas **(3)** and fed into a deposition reactor that contains heated silicon rods about (~10mm diameter) heated to an initial temperature of 400°C.



$$2SiHCl_3\ (g) + 3H_2\ (g) \rightarrow 2Si\ (s) + 6HCl\ (g) \quad \mathbf{(3)}$$

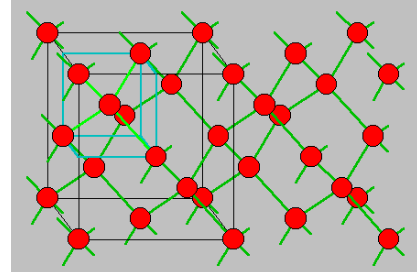
The silicon rods are ultra pure and serve as deposition sites for the silicon. Deposition lasts for 200 to 300 hours at a reaction temperature of ~ 1100 to 1200°C. The products of the deposition process are (~ 150 – 200 mm diameter) electronic grade (EG) silicon rods. The rods serve as the initial products for crystal growth processes such as the Czochralski process or the Float Zone method (Shimura, 1989).

Crystal Growth techniques: Unit Cell Structure

Properties of Solids:

Solids can be categorized into broad structural classes: (amorphous, polycrystalline and crystalline) based on the local and long-range arrangement of the constituent particles. Amorphous solids such as polystyrene (polymer), ceramics, glass, and silicon dioxide have no local uniformity or long range patter. The structure of EG-Si is polycrystalline, which means that there are some local arrangements of the silicon atoms (domains), but there is no long range, regularly repeating arrangement of these local domains. While the EGSi is of the correct purity, semiconductor technology requires a regular, repeating long-range arrangement of the silicon atoms: a crystalline structure. The positioning of the components in a crystalline structure is referred to as the crystal lattice. The smallest repeating unit of the crystal lattice is the unit cell, which describes the basic geometry of the lattice.

The physical and chemical properties of the lattice are repeatable, and predictable throughout the substance. Unit cells are parallelepipeds (a six sided polyhedron with parallelograms at each face) that can be classified based on the measures of their internal angles α, β, γ, and the length of their sides. August Bravais (1850) organized all possible unit cells into seven groups and 14 basic unit cells. The Bravais lattice groups can be used to predict all possible unit cell architectures. Bravais lattice groups include the triclinic, monoclinic, trigonal, hexagonal, orthorhombic, tetragonal, and cubic. (See Appendix C Bravais Lattices: for a listing of Bravais lattices). In addition to the geometry of a given unit cell, it is necessary to identify the spatial arrangement of atoms within each cell. Simple cubic (one atom per corner), face centered (simple cubic with an atom at each face) and body centered (face centered with an atom in the middle of the cell) are the more common arrangements (See Appendix D: Unit Cells). The silicon unit cell is characterized as a simple cubic cell with a diamond arrangement: two interpenetrating cubic cells forming a cell of eight atoms. Each atom is tetrahedrally bonded to another atom and each is located ¼ the distance from another along a major diagonal.



http://ece-www.colorado.edu /~bart/book/bravais.htm#diamond

Crystal Growth: Planar Orientation

In addition to the correct crystalline structure, the silicon crystal must possess the correct planar orientation. The Planar orientation is designated using Miller indices. The indices describe planes within the diamond lattice unit cell. (**See Text Box: Miller Planes for further explanation)**. The calculations of Atomic Density **(See Text Box: Miller Planes**) for each the (100, 110, and 111) planes show that atomic density is greatly affected by planar orientation. The implications of the atomic density on the surface of a miller plane are far reaching. Table 4 illustrates five physical characteristics that vary with atomic density. The available bond density closely follows the atomic density: the more atoms / cm^2 the more available surface bonds. The surface energy shows that a surface with high atomic and available bond density would be more "stable" and thus have a lower surface energy. Thus the (111) plane (highest atomic and available bond density) has the highest surface energy while the 100 (lower atomic and bond density) has the lowest surface energy. Young's modulus is a coefficient used to determine the elasticity of a substance (usually wires or rods). The elastic modulus measures the ratio of the strain (change in length) to the stress (the force acting on a body). In the consideration of the miller planes it follows that the 111 planes with a higher bond and atomic density would necessarily have a higher elastic modulus (Madou, Shimura 1998)

Table 4: Properties of the {100}, {110} & {111} Miller Planes

Property	100	110	111
Atomic density (10^{14}atom /cm^2)	6.78	9.59	15.76
a. Available Bond density *	6.78	9.59	11.76
b. Surface Energy J/m^2	2.13	1.51	1.23
c. Spacing	5.43	3.84	3.13
d. Young's modulus (dyn/cm^2)	1.3	1.51	1.9

* The density of available bonds for the reaction with H_2O molecules with consideration of steric hindrance; each silicon atom has in general two bonds capable of reaction.

(Shimura, 1989 p.48)

Given that efficiency of chemical reactions affects the manufacturing throughput, it is easy to understand that these physical and mechanical characteristics would have a profound effect on manufacturing decisions. Table 5 illustrates how crystallographic orientation affects ten fabrication processes. The profitatibility of a semiconductor facility depends on the number of wafers that are processed per hour (Benschop, 2002). With the rising cost of startup, and lithographic overhead, it is clear that fabrication facilities would exploit any variable that increased manufacturing throughput.

Table 5. Effect of Crystal Orientation on Fabrication Processes

	Crystallographic orientation		
FABRICATION PROCESS	100	110	111
Grown-Crystal Property	Good	Poor	Excellent
Growth Rate	Excellent	Acceptable	Good
Crystal Production Cost	Excellent	Poor	Excellent
Mechanical Strength	Good	Good	Excellent
Square Chip Dicing	Excellent	Acceptable	Acceptable
Radial Dopant Distribution	Excellent	Acceptable	Good
Oxidation Rate	Good	Excellent	Excellent
Oxidant Induced Stacking Fault	Acceptable	Acceptable	Good
Surface State Density	Excellent	Good	Acceptable
Epitaxial pattern displacement	Excellent	Good	Acceptable

Effects of Planar orientation on Fabrication Processes
Growth Rates.
The surface energy and atomic density of the crystallographic planes, predict that the growth rate for silicon would show a maximum in the {100} orientations and a minimum in the {111} orientations. (Shimura, 1989 p.50).

Thermal Oxidation rate is one of the most important manufacturing parameters in wafer fabrication. The {111} planes have a higher oxidation rate than the {100} planes given their greater atomic and available bond density. The increased oxide growth rate is easily understood, as there are more sites available for interaction. However the interface at the Si (crystalline silicon) and SiO_2 (amorphous silica) boundary is a transition area that contains two areas of trapped charge density. The 111 planes with a greater bond and atomic density have necessarily higher trapped charge values than the {100} planes: (lower bond/atomic density implies lower trapped charges. As a result the {100} orientation is preferred for IC circuit technology as trapped charges are undesirable in the fabrication of MOSFET transistors.
Etch rates:
Etch rate is a function of the surface free bonds. This increases with the number of surface free bonds. As atomic density and available bond density increase, the etch rate decreases as surface reactions have more interactions to overcome. This relates to the overall stability of the plane. The 111 plane with greater atomic density and bond density is in effect more stable. Thus etching would occur at a faster rate on the less stable 100 plane. Etch rates in a water ethylenediamine solution are 50: 30: and 3 um/hr for the 100, 110 and 111 planes respectively. (Shimura p.49).

Text Box: Miller Planes

In order to determine the family designation of a given crystallographic plane, one must first determine where the plane intersects the crystallographic axes labeled x, y, z in figure 1. The distance of these intersects from (an) origin are noted. If a plane does not cross an axis, the symbol ∞ is used to denote no intersection. Once noted, the reciprocal of each intercept is taken so as to remove any fractional intercepts. (See figure 4). These numbers are then noted as the Miller Index for a given plane.

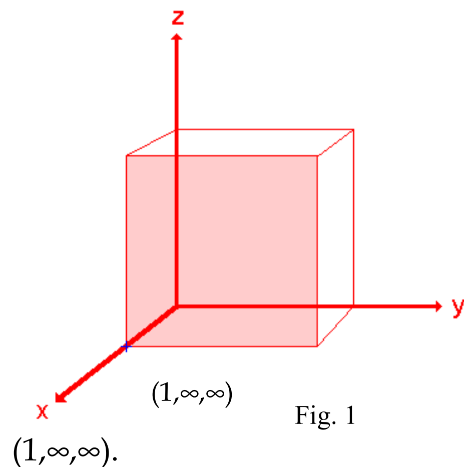
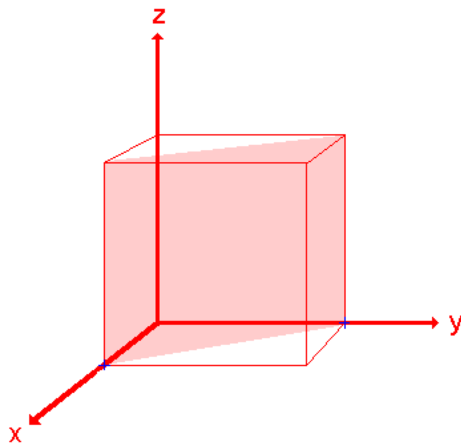


Fig. 1

(1,∞,∞).

Calculating the (100) Plane

The plane intersects the x axis at 1: there is no intersect at the z or y axes; their intersects are noted with ∞. The intersects of the plane are (1,∞,∞). The reciprocals of these intersects are (1/1 =1,1/∞ = 0, 1/∞ = 0).



Calculating the 110 Plane

The 110 Plane intersects the crystallographic axes at (1,1,∞). Reciprocals are (1/1, 1/1, 1/ ∞): Miller index is (1,1,0)

http://www.mse.ufl.edu/~jambr/EMA3010/miller_indices.pdf

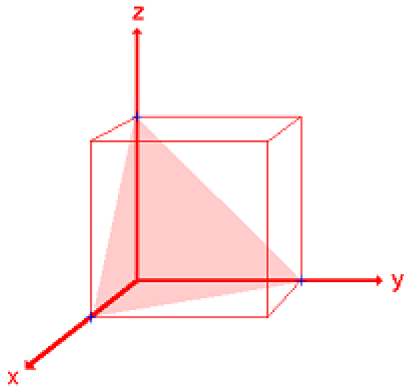


Fig.3

Calculating the (1,1,1) Plane

Plane intersects crystallographic axes at (1,1,1). Reciprocals are (1,1,1). Miller Index is (1,1,1)

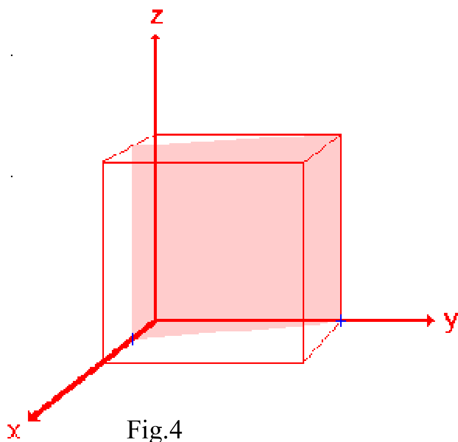
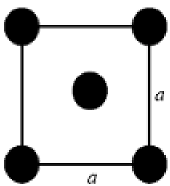


Fig.4

Calculating the (2,1,0) Plane

Plane intersects are (1/2,1, ∞). Reciprocals are 1/1/2, 1/1, 1/∞: Miller index is (2,1,0)

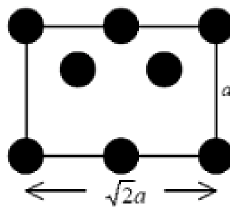
Atomic Density Calculations in The Miller Planes



Density in the 100 Plane:

$$\frac{2atoms}{(5.43^{-8}cm)^2} =$$

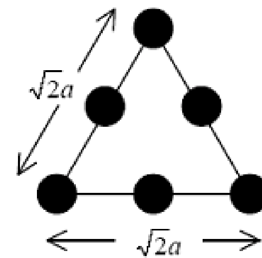
$$6.78E^{14}atoms/cm^2$$



Density in the 110 Plane

$$\frac{4atoms}{\sqrt{2}(5.43^{-8}cm)^2} =$$

$$9.60E14atoms/cm^2$$



Density in the 111 Plane

$$\frac{2atoms}{\frac{\sqrt{\frac{3}{2}}(5.43^{-8}cm)\frac{\sqrt{2}}{2}(5.43^{-8}cm}{2}}$$

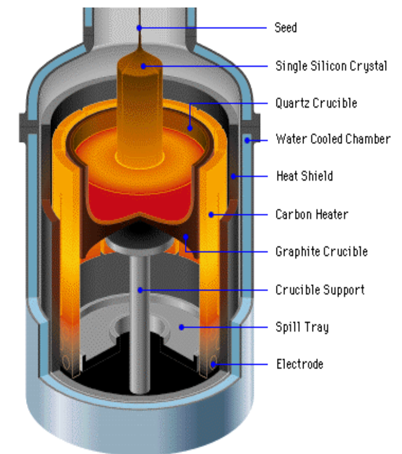
$$15.74E14atoms/cm^2$$

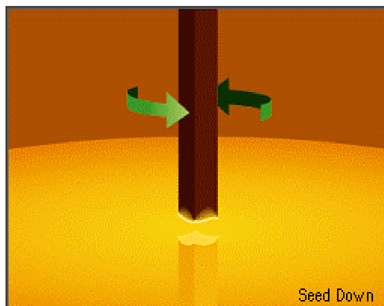
Crystal Growth: Czochralski Process

Although the EGSi is ultra pure, it is a polycrystalline material which does not possess a precise crystalline structure as required by semiconductor technology. Crystal Growth processes "grow" crystalline silicon ingots with the prescribed planar orientation. There are currently three accepted methods of crystal growth: (The Bridgeman technique, the Float Zone method, and the Czochralksi process. Of these three, the preferred method is the Czochralksi process as it can more easily produces 300 mm diameter wafers currently used in today's semiconductor fabrication procedures. Larger wafers increase productivity, lower costs, and increase profits because more chips (processors) can be manufactured on a large wafer surface. Batch processing can produce as many as 100 microprocessors on a single wafer. Throughput efficiency and profitability are major concerns given the enormous startup cost of fabrication technology and manufacturing facilities. This economic incentive has helped create the need for an increase in wafer diameter. The Czochralski process has become the favored process, as it has proven successful in the manufacturing of wafers of ever increasing diameter.

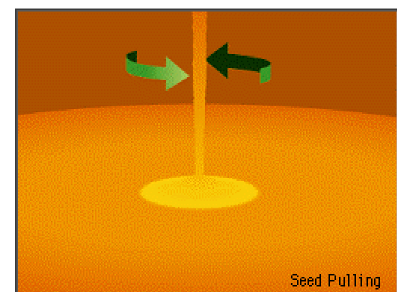
Jan Czochralksi (1885 – 1953) developed this method in 1916 to grow single crystals of metals. Although G.K Teal and J. B. Little of Bell Labs perfected the method to grow germanium crystal in 1950, the Czochralski name remains.

The Czochralski process grows large ingots (boules) of single crystal silicon. The ingots are approximately 400 mm in diameter and 1 – 2 meters in length and weigh up to 300 kilograms. To make the ingots, large chunks of polycrystalline EGSi are placed into a reaction crucible made of fused quartz and heated to a temperature of 1421 ^oC. An inert gas such as argon is back fed into the crucible to help reduce crystallographic defects, as the boule is grown. Once the polycrystalline silicon is melted, dopants are added to the melt to produce the desired electrical properties.

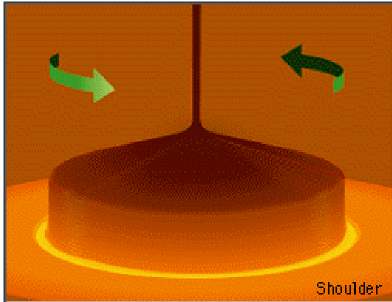




To create the proper crystalline structure, a seed of (~0.5mm diameter / 100-300 mm long with the correct crystal and planar orientation) is attached to a pull rod and lowered into the melt. Once melted, the seed is slowly pulled from the melt at controlled pull rate. The pull rate is a critical variable in the control of the diameter and crystallographic purity of the ingot. Two types of defects affect the crystallographic purity: vacancies (atoms missing in the lattice) and interstitials (non bonded atoms within the lattice). The ratio and concentration of these micro defects within the silicon ingot is a function of the temperature gradient at the melt/crystal interface. This thermal gradient is affected by the pull rate. The range of

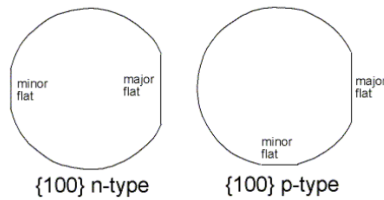


pull rates is determined by the many factors that vary among the many Czochralski operators. Experience is a major variable. Pull rates vary from as high as (0.8-2.0 mm/min), medium (0.5-0.8 mm/min) to low (less than 0.5 mm/min.



In order to control the thermal variables that exist at the melt / seed crystal interface, as well as the temperature variances within the crucible, both the seed crystal and the melt are rotated. The seed crystal rotates counterclockwise (at a higher rate) and the melt rotates in a clockwise manner. The rotation helps to reduce thermal asymmetries that tend to destabilize the growth of large diameter wafers.

Once the boule is grown, the top and tail of the boule are removed. The ingot is thence shaped to the proper diameter. Orientation flats that describe the doping and planar orientation of the crystal are ground into the ingot. The ingot is etched to remove any defects from grinding and shaping.



Wafers are sliced from the ingot, using a diamond saw blades. The edges of the wafers are chemically etched to remove any surface damage; they are then polished and packaged for distribution to semiconductor fabrication facilities.

Text Box: Diffraction and the Rayleigh Criterion

Diffraction is a phenomenon that occurs when waves (electromagnetic, water, or sound) bend around the corners of a sharp edge or spread out as pass through a small opening. An example of diffraction is observed when water waves seem to bend around large rocks in a pond or lake. As the waves encounter the obstacle, they spread out in all directions and some waves "bend" around and spread into the shadow region behind the rock. In order to investigate the effect of diffraction on the resolution of optical systems, we will investigate the diffraction that occurs when light passes through a single small opening. Diffraction through an opening is a function of the size of the opening (D) and the wavelength of light (λ). If the opening is smaller than the incident wavelength, light waves will spread out through the opening and diffraction will occur. As waves spread beyond the opening, they do so at a variety of angles (θ). Pairs of diffracted waves can interact with each other in two distinct ways. They can interact with each other in phase (crest to crest: constructive interference) or out of phase (crest to trough: destructive interference). Waves 1 and 2 in Figure 2 illustrate constructive interference; waves 3 and 4 are examples of destructive interference. Figure 3 shows the relationship between the angle of diffraction and the slit width. If the distance $d\sin\theta$ is equal to λ, the waves will interfere destructively. Thus destructive interference occurs when $d \sin\theta = \lambda$ (**1**) . This is also true for any whole number multiple of wavelengths so that minima occur whenever $d \sin\theta = (m)\lambda$ (**2**): m = 1, 2, 3, (Smith, 1998,p.187). When θ is very small $\sin\theta \sim \theta$; thus equation 1 can be written as $d\,\theta = \lambda / D$ (**3**) or $\theta = \lambda / D$ (**4**).

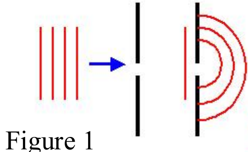


Figure 1

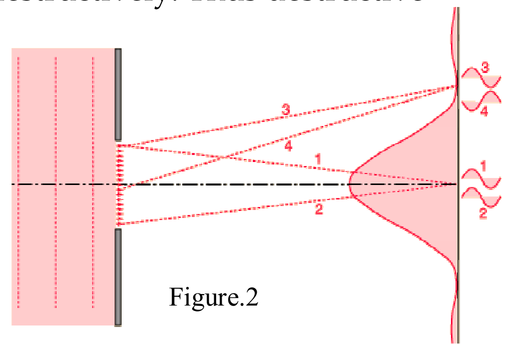
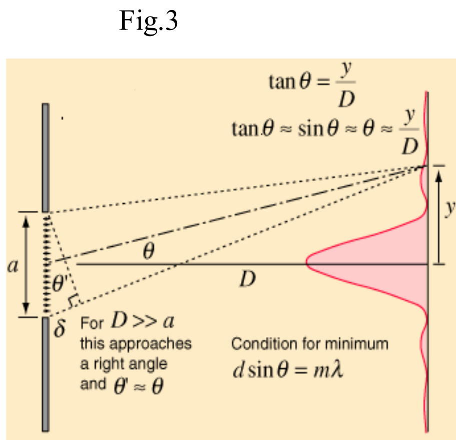


Figure.2

Fig.3



Diffraction Through a Lens or Circular Opening

The resolution of a lens (or a circular opening) is a measure of its ability to produce distinct images of 2 closely spaced point objects. A lens with a high resolution will show closely spaced objects as separate images. Figure 4 shows the images formed by lenses with different resolutions. The images to the far right are resolved, those in the middle and far left are not. Note that the images have a bright central area (the Airy disk) surrounded by circular fringes. This diffraction pattern is the result of the light passing through the lens rather than a rectangular slit. The average diameter of a lens of diameter D is (D/1.22) (Giancoli 2002,p 775).

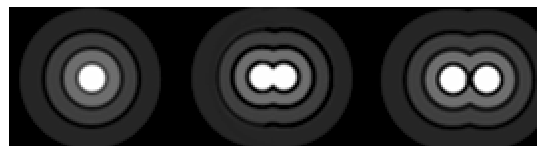


Fig.4

Using this value in equation 4 gives minima for this diffraction pattern at

$$\theta = 1.22\, \lambda / D. \quad \mathbf{(5)}$$

Rayleigh Criterion

The resolution of two images is determined quantitatively by the Rayleigh Criterion, which states "two images are just resolvable when the center or the diffraction disk of one is directly over the first minimum in the diffraction pattern of the other," (Giancoli, 2002, p. 776).

The middle image in figure 5 shows illustrates this limit to resolution. The maximum of the diffraction pattern of one image is directly over the minima of the other. Under these conditions, the two images are not resolvable.

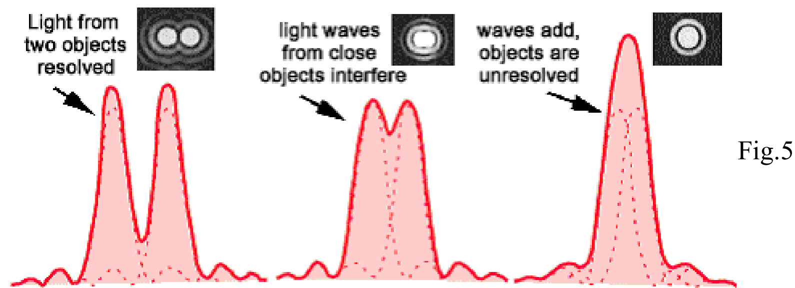


Fig.5

Equation 5 can be used to determine the Resolving Power (RP) of an optical system such as a microscope (or a semiconductor projection system). In optical geometry, equation 5 can be rewritten using the angle of acceptance of the objective lens (α) of the optical system. In terms of the angle of acceptance, D = 2 sin α. Using this value of D in equation 5, the resolution (RP) can be rewritten as:

$$\text{RP} = \frac{1.22\lambda}{2\sin\alpha} = \frac{0..61\lambda}{\sin\alpha} (6)$$

The refractive index of a lens (n) reduces the wavelength λ by a factor of $\frac{n}{\lambda}$. Equation 6 is then rewritten as RP = $\frac{0.61\lambda}{n\sin\alpha} (7)$. In optical systems n sinα is defined as the Numerical Aperture (NA) of the lens (Campbell, 1996). Placing this term in equation (7) yields the Resolution Equation for the optical exposure systems used in semiconductor projection systems. Thus the resolution (RP) of the system is given by:

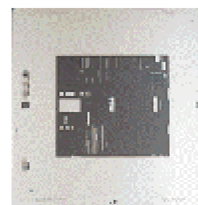
$$RP = 0.61\frac{\lambda}{NA} \quad \mathbf{(7)}$$ (Benschop, p.19; Campbell, p168).

References:

Figure 2: http://230nsc1.phy-astr.gsu.edu/hbase/phyopt/imgpho/sinslitwid.gif
Figure 3: http://hyperphysics.phy-astr.gsu.edu/hbase/phyopt/fraungeo.html
Figure 4 http://nsm1.fullerton.edu/~skarl/EM/Microscopy/Resolution.html
Figure 5: http://www.xenophilia.com/zb/zb0012/RayleighCriterion.gif

Microlithography: Patterning of Silicon Substrate

A software engineer designs the functional logic of a microprocessor or memory chip. The circuit designer creates the circuitry of the processor from existing layout rules that determine parameters such as feature size, line width, minimum feature overlap between layers, and all critical measurement tolerances. The integrated circuit is assembled and checked to insure proper functioning at which time a layout of the circuit is generated. Given that semiconductor circuitry is fabricated one layer at a time, the circuit layout must separate the circuit design into individual layers. The number of layers in silicon fabrication can vary from 15 –20 layers, some processes can require up to 28 layers of design. Each layer of the design is digitized and used to create a photomask of the particular circuit layer. Photomasks are made using metal (usually chrome) to recreate the circuit pattern on glass that has a high degree of optical purity and transparency with a small thermal expansion coefficient, and a highly polished surface that will not scatter light. Masks are designated as 1X (the image size on the mask is the same as the final feature), or reducing masks (5X or 10X). The features in the photomask are projected onto the surface of the wafer that has been coated with a layer of photoresist. Upon exposure, the pattern in the mask is imprinted in the photoresist. The pattern thus imprinted upon the silicon surface exposes selected areas of the silicon wafer to a variety of fabrication procedures. (Please refer to the fabrication process for the n-MOS transistor in appendix A for an example of these selective processes.).



Chemistry of Photoresists

Photoresists are compositions of polymers and light sensitive materials that resist the action of chemical used during the fabrication process. Photoresists are classified according to their response to optical energy. A negative resist polymerizes upon exposure to light while positive resist becomes more soluble upon exposure. The photoactive component of resists is an additive that promotes the differential responses to light. In a negative resist the photoactive compound promotes cross branching between the polymer chains, while in a positive resist the photoactive compound promotes solubility during the developing process. Negative photoresists were the first resists used in the semiconductor fabrication, however as feature size and line width decreased, they were replaced by positive resists. Positive photoresists are preferred for the following reasons

- They have a higher aspect ratio:
- Negative resists have a poor reactivity to light below 436 nm
- Positive resists absorb all Hg lines (365, 405, 435nm)
- Positive resists do not swell upon exposure
- Positive resists are not oxygen sensitive

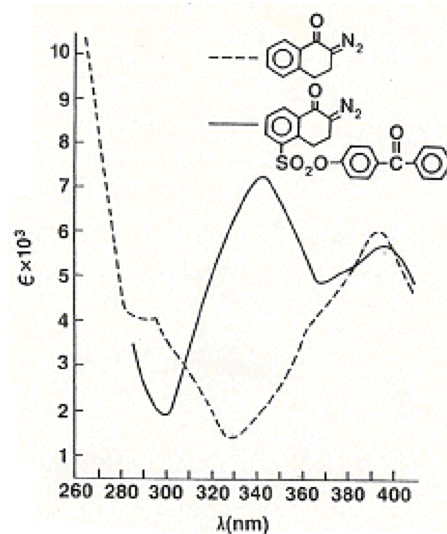
Positive resists are generally composed of a resin type polymer, a photoactive compound and other additives that control for properties such as adhesion and thermal stability (Moreau, 1988). Table 3 is a typical DQN formulation. The DQN resist is composed of a meta cresol polymer (a Novolak resin) (Figure 1 Appendix E) complexed with Diazoquinone (Figure 2 Appendix E).

DQ	2 grams
Novolak	8 grams
Cellosolve acetate	20 grams
Butyl acetate	2 grams
Xylene	2 grams
Water (trace)	0.05grams

Moreau, 1988 p. 43

Photochemical reaction of DiazoQuinone:

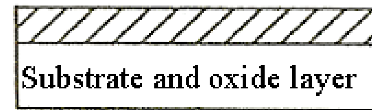
Figure 1 shows that DQ absorbs 365-435 nm (mercury lines). The graph in Figure 1 shows the absorbance of DQ. Note that a substitution at the para position greatly enhances the absorbance. Approximately 100-200mJ/cm^2 (Moreau, 1988) are needed to fully photosensitive the diazoquinone. Upon exposure to light, the diazoquinone loses the N_2 molecule to form a carbene, which rearranges to a ketene via the Wolff rearrangement. The ketene reacts with trace water in the resin to form the final product (3-indenecarboxylic acid), which is soluble in alkaline solutions. (Figure 3 Appendix E) shows the Novolak resin complexed with the DQ via hydrogen bonds at the carbonyl oxygen. Thus when the indencarboxylic acid reacts with an alkaline developer such as (TMAH: tetramethylammonium hydroxide), the attached Novolak can be rinsed away along with the developer. Once the developer is rinsed, chemical etching will remove the exposed areas for a series of manufacturing processes. In the example that follows, the source and drain regions are doped with phosphorous to produce n regions. The following section presents the subsequent steps in the production of the MOSFET. It is meant to be representative as a comprehensive account of all of the remaining fabrication processes is beyond the scope of this paper.



Moreau,p.39

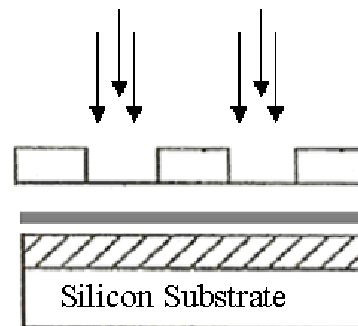
Metal Oxide Semiconductor Fabrication Process

A layer of silicon oxide is grown onto the silicon substrate. The substrate is p-doped silicon. This is the first of several insulation layers. The oxide is "grown" by placing the wafer in reaction chambers with either gaseous oxygen (dry oxidation) or steam (wet oxidation). The insulation provides an electrical barrier and protects the wafer.

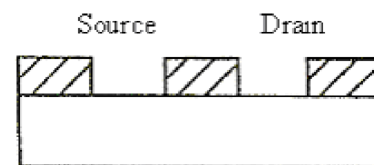


A layer of positive photoresist is applied to the wafer. The resist is spun applied to assure adherence and even coating of the wafer

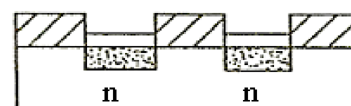
The resist is soft baked to evaporate the solvent and set the edges. A photo mask is aligned upon the wafer and exposed with light of the appropriate wavelength. The nature of the resist is such that exposed areas become more soluble in the presence of an alkaline developing solution.



The wafer is developed so as to remove soluble resists. A second bake sets the pattern into the resist. An etching agent is used to remove the oxide in the drain and source areas of the transistor.

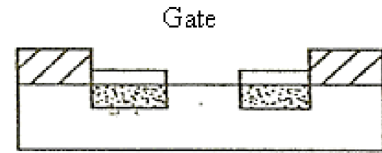


This is followed by ion implantation of pentavalent phosphorous atoms so as to create the n doped region. A second layer of oxide is grown so as to insulate the drain / source regions.

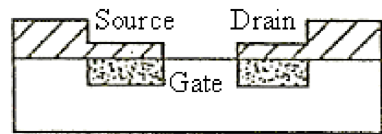


N doping and re-oxidation of source and drain openings

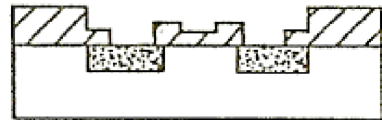
Gate oxide is grown



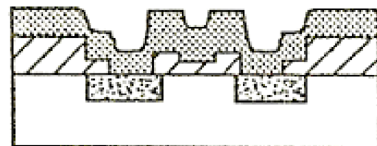
Patterning and etching removes oxide in gate region: the gate region is formed.



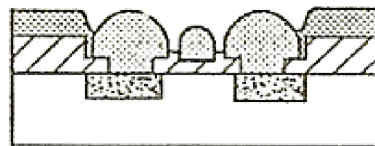
Contact holes for metal contacts are patterned into source, drain and gate regions.



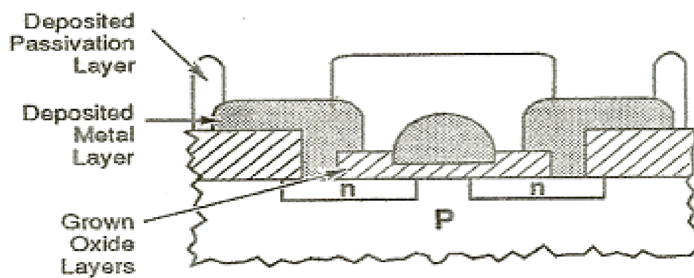
Conducting metal is deposited on wafer



Metal is patterned and alloyed to wafer



Completed Metal Oxide Semiconductor Transistor



Van Zant p.88

Limits to Optical Lithography

Gordon Moore's prediction that the density of integrated circuits would double every 18 months has been maintained for the past 30 years. (Benschop, 2002). The motivation to create ever more dense circuits has been fueled by ever growing profit margins and the public demand for smaller, more efficient and economical digital devices. There are however limits to the ever shrinking transistor.

The projection system used in the exposure of photomasks creates a diffraction pattern, which limits the resolution of the projected images. Equation 7 from the textbox: **Diffraction and the Rayleigh criterion** set the limit of the process factor k_1 at 0.61

$$RP = 0.61\frac{\lambda}{NA} \quad (7)$$

(Benschop, p.19; Campbell, p168).

Table 6 illustrates how given manufacturing variables such as the wavelength of radiation, the numerical aperture of the lens system and the process factor (k_1) can be used to determine the process limits (the minimal distance between equal lines and spaces on the silicon wafer) of a given fabrication process. For example, the process limits for a process using the i-line radiation from a mercury arc lamp (a λ of 335 nm), with a lens numerical aperture of 0.65 sets and a process factor of k_1 = 0.61 would have a minimal resolution of

$$RP = \frac{0.61(335E^{-9})}{0.65} = 342nm \quad (8)$$

Table 6. Application Range and limits to Optical Lithography

Optical lithography systems					
Wavelength NA		**365nm**	**248**	**193**	**157**
Source		**i-line**	**KrF**	**ArF**	**F_2**
NA (Numerical Aperture)		**0.65**	**0.63-0.80-**	**0.63-0.85**	**0.70-0.85**
Method	**Process factor K_1**				
Conventional Stepper	**0.60**	**335**	**285-185**		
+Off axis Illumination	**0.50**	**280**	**195-155**	**155-175**	**110-90**
PSM and /or Strong OAI + OPC	**0.40**		**175-125**	**125-90**	**90-75**
Thin layer imaging	**0.30**		**120-90**	**90-70**	**70-55**
Physical limit equal lines and space	**0.25**	**140**	**100-75**	**75-55**	**55-45**

(Luryi, 2002 p.20)

A 342 nm resolution sets the pitch (sum of equal lines and spaces at 684) nm, with minimal line/ feature size at 342 nm (Campbell, 1996).   A ~700nm pitch process was used in the late 1980 with an i/g line exposure process. The projected process for the current generation is for 65nm and below.

Table 1: Wavelength "Generations"

Year	Node	Lithography
1981	2000nm	i/g-line Steppers
1984	1500nm	i/g-line Steppers
1987	1000nm	i/g-line Steppers
1990	800nm	i/g-line Steppers
1993	500nm	i/g-line Steppers
1995	350nm	i-line ➔ DUV
1997	250nm	DUV
1999	180nm	DUV
2001	130nm	DUV
2003	90nm	193nm
2005	65nm	193nm ➔ 157nm
2007	45nm	157nm ➔ EUV
2009	32nm and below	EUV

http://developer.intel.com/technology/itj/2002/volume06issue02/art06_lithographyroadmap/vol6iss2_art06.pdf

The three additional process factors in Table 6 are improvements to the 0.61 limiting process factor. Each one of these modifications (Off Axis illumination, PSM or Strong OAI, and Thin Layer Imaging) is meant to improve the process factor by addressing a different distortion produced by the optical exposure system. Lithographic technicians use these enhancements in an attempt to improve the resolution of a given set of process variables. Equation 7 above can be used to verify the limits of any given set of process variable. It should be noted that the enhancements are limited to certain wavelengths of energy. The use of exiplex lasers ArF and KrF, and the eximer laser F_2 has extended the limits of resolution to the 55 nm process range, however as we proceed into the sub 55 nm range, it is clear that "next generation lithography (NGL) (Benschop, 2002) will be needed as optical lithography has reached its limit. The (NGL) includes processes such as Electron Beam projection lithography, Ion Beam projection lithography, X-ray and Extreme ultraviolet lithography. These are the frontiers of lithography that of our next generation of digital electronics will have to cross.

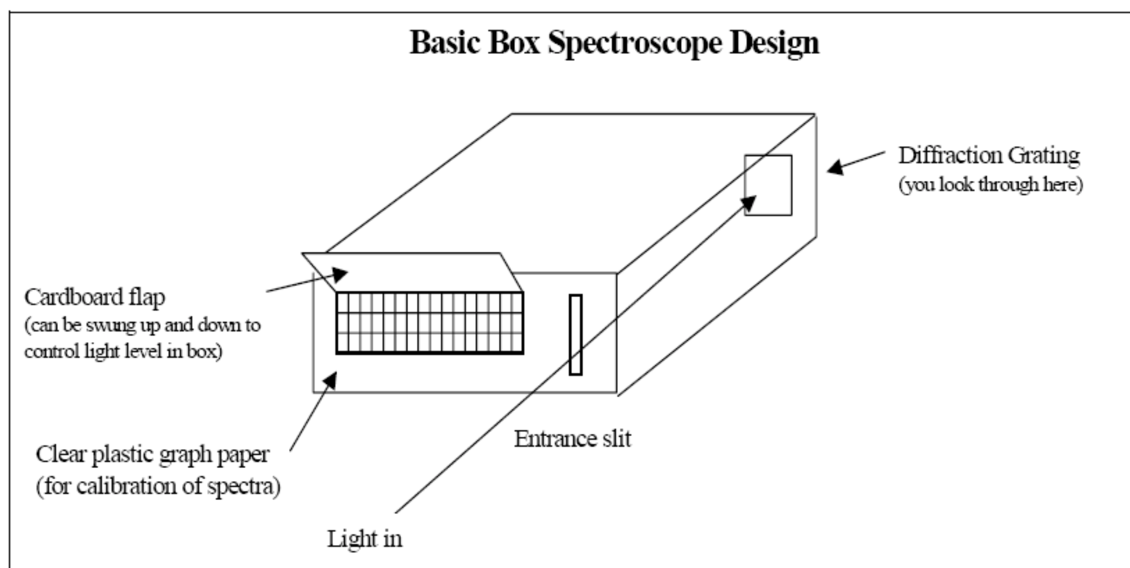
Pizza Spectroscope Activity

In this laboratory you will build your own pizza box spectroscope. You will calibrate your spectroscope and thence use it to observe the emission patterns of a few elements. You will end the activity by determining the wavelength of light from a small laser. You will need to use some basic mathematics and your understanding of diffraction patterns in order to complete this laboratory.

You will need to bring in a small pizza box from home. A box for a small personal pizza is best. Your teacher will provide scissors, tape, graph paper and the diffraction grating. Use the diagram below to construct your spectroscope.

How to Assemble Your Spectroscope

Cut a hole for the grating and slit. If your box is not square, use one long side for the slit, and the other for your grating. These do not work well on the short sides. Use the diagram below as a guide. When you've finished your spectroscope, look up at the fluorescent lights. You should see a spectrum (a rainbow) on the side of the box. If you don't see a spectrum, rotate the grating 90 degrees. Mark the position of the spectrum in the box; this is where you will cut your flap (see the flap in the diagram!). Mark where the spectrum starts and ends and then cut a flap on three sides slightly wider than this area so that you can attach transparent graph paper scale later (see diagram). Do NOT mount the transparent graph paper at this time**.** Next place strips of black tape on either side of the entrance slit you cut in the box. Use the tape to narrow the slit to approximately 1 mm wide. Show your completed spectroscope to your teacher before you continue with the activity.



Calibrating the Spectroscope

Number the lines on your graph paper scale. You need not number every line, just enough so that you know the number of each one (i.e. 1,2,3,5, 8,10,etc),
Then Tape the graph paper to the inside of the spectroscope where you saw your spectrum. Make certain you can see the numbers of your graph and the spectrum.
Now aim your graph at the mercury lamp. You should see four bright lines on your spectrum and on the graph. Notice where the lines are on the graph and write down the number that corresponds to each line you see. Use at least one decimal place for the location of each line on your graph: (i.e. 3.4 or 5.8,etc.). You should see a dark violet, a bright blue, a bright green and a bright yellow line. You may see other faint lines, but the bright ones should be enough to calibrate your instrument (It may be difficult to see the violet line). Make certain to have at least three lines on your graph. Try to get sharp lines on the graph. You may need to adjust the width of your entrance slit, or block out any excess light that seeps into your spectroscope.
The following table has the positions of the Hg lamp lines. Use these numbers and their location on your spectroscope's graph to make a calibration graph. The graph will be used to determine the position of the lines you observe later in this activity.

Color	Wavelength	Position on Spectroscope Graph
Dark violet	404.7 nm	
Bright blue	435.8 nm	
Bright green	546.1 nm	
Bright yellow	579.0 nm	

Make a graph of the positions of your spectroscope lines versus wavelength. Draw a best-fit line. The line should be evenly spaced from all your point. This graph is your calibration graph.

Observing Spectra

To begin you will observe the spectra of three emission tubes in the class. Write down the color and location of the lines you observe.

Next observe the emission from a hydrogen tube. Write down the color of the brightest lines along with their location.

Use your calibration graph to determine the wavelength of the hydrogen emission lines. Compare your values to the accepted values. (These will be on the lab whiteboard). Use the accepted values and your observed values to determine the percent error of you spectroscope.

You will be assigned one of several discharge tubes. Your task will be to figure out what element you are observing. Observe the emission, calculate the wavelength, and adjust using the percent error of your spectroscope.

Next you will observe the emission spectra of metals. This will require that you work with a partner. Solutions of the salts of five metals are located on the materials bench. Place one of the prepared splints into the flame of a Bunsen burner. Record the color you see without using the spectroscope. Repeat this using the spectroscope. Note any emission lines that you see. Once again use your graph, the error correction and submit a guess for your metal.

Do you note any difference in the spectra of the metals and those of the discharge tubes?

Once completed, plot your calibration curve using the excel program. Use the program to determine the wavelength of the lines you observed. Are there any discrepancies between your data and the Excel data?

Assessment Questions:

1. The Silicon Unit Cell has a diamond cell structure, a face centered cell with 4 internal atoms. Calculate the amount of space that is occupied by the atoms and the empty space within the cube. The edge of the diamond cell is 5.43 A; the radius of the atom is 1.12 A.
2. The wavelength of light emitted by an LED is λ = 580 nm. What is the energy of this light in eV and in Joules, and kJ/mole?
3. The materials listed in Table are able to function as Light Emitting Diodes. Which semiconductors are missing? Why can't we use these materials as LED? You will need to search the source provided in the references.
4. Compare the atomic density and available bond density of the (100) and the (111) planes. Which plane has the greater oxidation rate? Explain why using the atomic and bond density.
5. What is your opinion of our dependence on computers? Do you think that our society is too dependent on them? What about you? What do you think of all the information that we can access via the Internet: Do you think it has a positive or negative affect on your life?

Solutions

Problem 1.

The diamond cell has 8 (1/8 atom per corner =1 atom: 6 face centered atoms ½ atom per face = 3 atoms, and 4 interleavened atoms = 4 atoms. Total is 8 atoms per cell. The atoms touch along a body diagonal equal to $\frac{\sqrt{3}a}{8}$. Thus the space occupied by the atoms is $\frac{4}{3}\pi r^3(8atoms)$ divided by the volume of the sphere which is $\left(\frac{\sqrt{3}a}{8}\right)^3$. This equals $\frac{\pi\sqrt{3}}{16}=0.3400$ or a 34% packing density. The empty space is therefore 66% of the cell.

Problem 2 Solution:

$$E=(\frac{hc}{\lambda})=(\frac{(6.626E^{-34}Js)(3.00E^{8}ms)}{580E^{-9}m})=3.43E^{-19}J:\ \frac{3.43E^{-19}J}{1.60E^{-19}eVJ^{-1}}=2.15eV$$

3.43E-19J per photon X 6.02E23 photons per mole = 206 kJ/mole. Refer to Appendix F for more LED band gap values.

Problem 3.

The listed semiconductors are not intrinsic, and they have direct band gaps. Silicon and germanium have indirect band gaps. When electrons in silicon / germanium are

promoted to the conduction band, both their energy and momentum are changed. Given that both energy and momentum need be conserved. When the electron returns to the valence band, the conservation of both momentum and energy is achieved by the creation of quantized lattice vibrational energy in the form of phonons. The phonons emit the absorbed energy in the form of heat, not visible light. Thus silicon and germanium are poor choices for Light Emitting Diodes.

Problem 4 solution:

The 111 planes have a greater bond and atom density than the 100 planes. This greater density gives them a lower surface energy as the increased number of atoms and bonds make them a more stable surface. The same reasoning explains the higher oxidation rate.

Problem 5:

This is an open-ended essay question. There is no correct answer for this question, however students must give at least three reasons that support each of their opinions. At least one of the supporting reasons must be quantitative.

Question:

Why can you see the light in some diodes but not in other diodes?

Existing Information: Semiconductors listed have direct band gaps: silicon / germanium have indirect band gaps, thus they are not suitable for photon emissions.
Diodes exploit the particle nature of light as photons are emitted.
Electrons in the conduction band are "reunited" with holes in the valence band.
http://cnx.rice.edu/content/m1011/latest/

Results

A. LED emits light in the visible range of EMS, the other diode emits somewhere from IR and below probably not in the UV or higher
B. Ga/As (Band gap1.43eV) is used in remote controls: Ga/Al/P(Band Gap1.95) is for LED.
C. The wavelength of the 1.43 gap is 863nm: the 1.95 is 633.

Reflect and Organize

A. If light is emitted in the LED what kind of energy is emitted in the remote control diode?
B. What is there about the semiconductor that could produce light energy?
C. What kinds of equations do we need for this calculation?

Peer Review

A-B> If A is true, then what are the structural differences in the two types of diodes?
B-C. The band gap energy relates to the kind of energy emitted, so we can calculate the energy of the emission from the band gap energy?

Information Needed

Electromagnetic Spectrum
List of Semiconductor materials with their properties
Equations: $E=h\nu$: $c=\lambda\nu$: conversion factor for eV to Joules: Planck's constant and speed of light.

Can you determine the band gap for LEDs of different colors?

The size of the Band gap energy determines what kind of energy the diode emits.

Communal Knowledge

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Van Zant, P., Microchip Fabrication: A Practical Guide to Semiconductor Processing 2nd Edition, McGraw Hill Publishing, New York, 1990.

Web Resources:

Hyper physics web site: *http://hyperphysics.phyastr.gsu.edu/hbase/solids/band.html#c1*

Internatiiona Technology Roadmap For Semiconductors Lithography
http://public.itrs.net/Files/2000UpdateFinal/Lithography2000final.pdf

Intel Lithography RoadMap
http://developer.intel.com/technology/itj/2002/volume06issue02/art06_lithographyroadmap/vol6iss2_art06.pdf

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http://www.mse.ufl.edu/~jambr/EMA3010/miller_indices.pdf

Crystal Orientation and Reactivity:
Madou,M, Si crystal growth, Si crystalorientation, oxidation and interface defects-. Web Document at:
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PIM Resource: Wilson, B. Light Emitting Diodes. Web resource at:
http://cnx.rice.edu/content/m1011/latest/

Table 1 source: Data Source:
http://www.intel.com/pressroom/kits/quickref.htm

Cover picture credits
Point Contact Transistor
http://www.icknowledge.com/history/pointcontacttransistor.gif

Transistor Mighty Mite of Electronics
http://www.creighton.edu/~davereed/csc107.S02/Images/transistor.jpg

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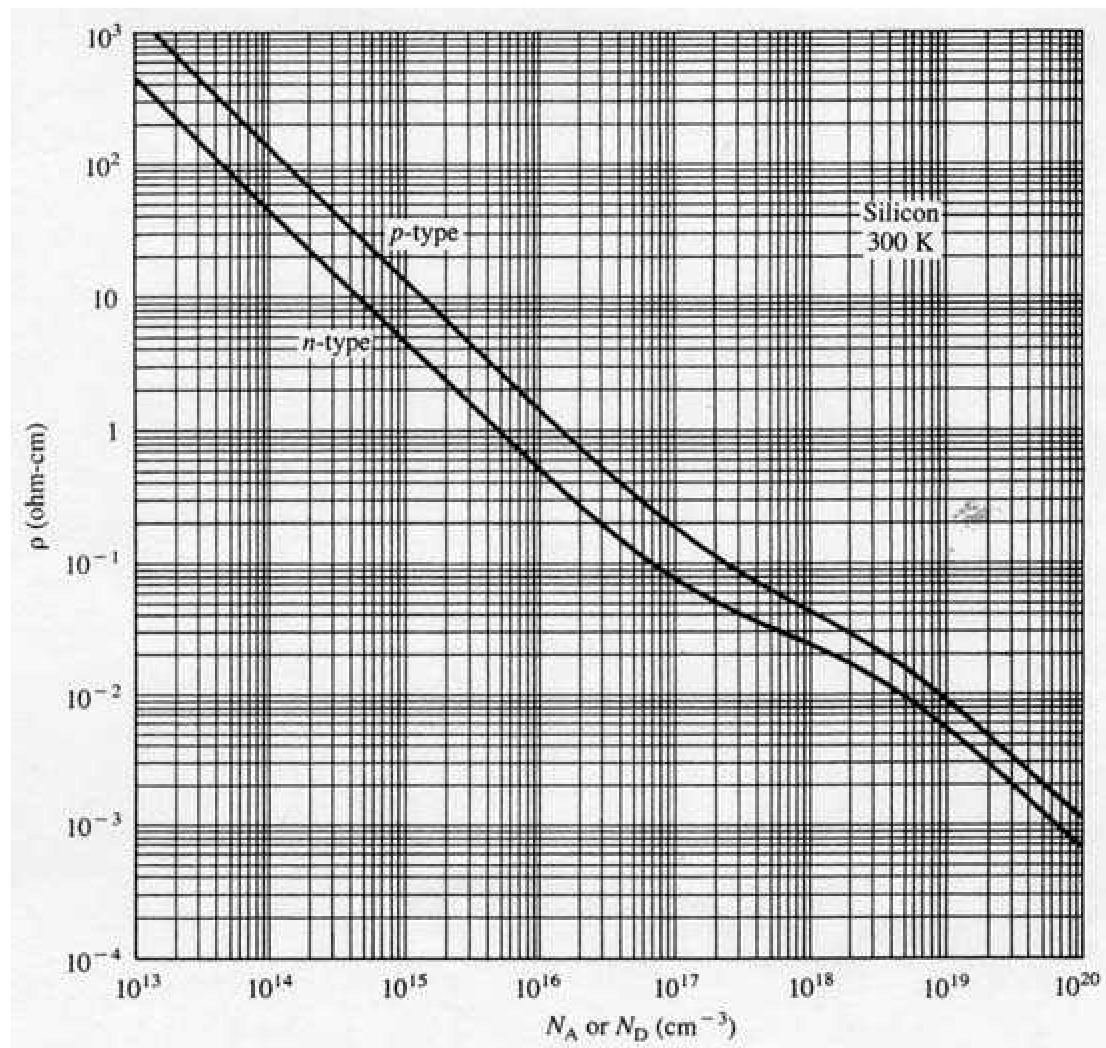
Intel gate Transistor
http://developer.intel.com/technology/itj/2002/volume06issue02/art06_lithographyroadmap/vol6iss2_art06.pdf

APPENDICES

APPENDIX A: ENIAC STATISTICS

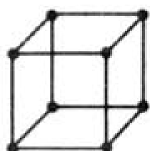
The ENIAC computer is one of the earlier computing devices. A modern hand held calculator costing ~ $15.00 has more computing power. The following are the ENIAC statistics:
17,468 vacuum tubes
70,000 resistors
10,000 capacitors
6,000 relays
150,000 watts required
450,000 (1940) dollars
30X 50 feet
30 tons
Reliability: 5.6-hour average

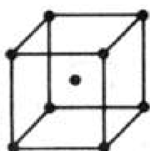
Appendix B:
Table 2 Resistivity Graph

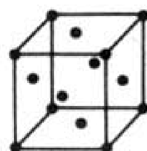


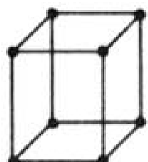
Van Zant, p.29

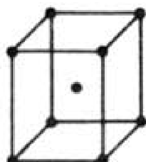
Appendix C Bravais Lattices


Simple cubic


Body-centered cubic


Face-centered cubic


Simple tetragonal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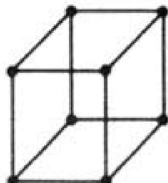
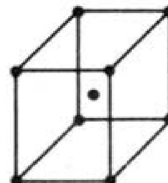
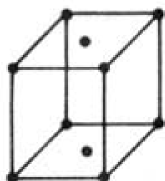

Simple orthorhombic


Body-centered orthorhombic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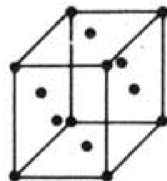
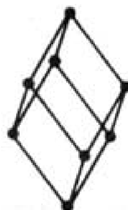
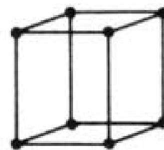
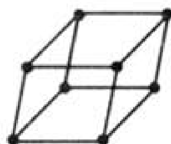
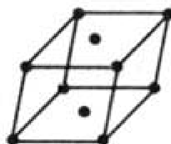
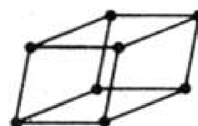

Face-centered orthorhombic


Rhombohedral


Hexagonal

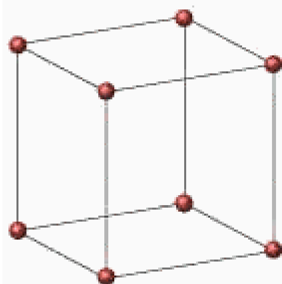

Simple monoclinic

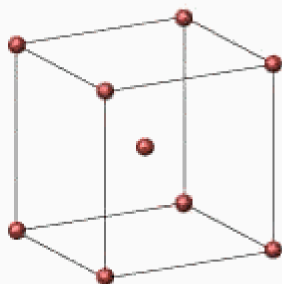

Base-centered monoclinic

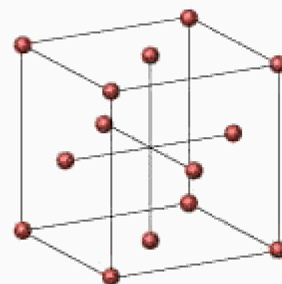

Triclinic

http://www.metal.or.kr/college/m_basic/xyl/s61-1.jpg

Appendix D: Cubic Unit Cells

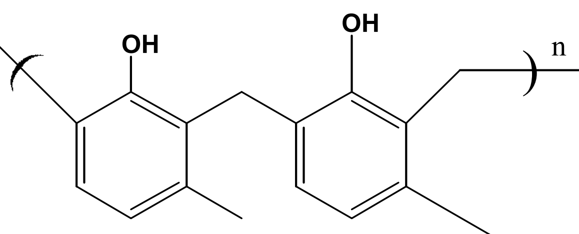

Primitive cubic


Body-centered cubic


Face-centered cubic

http://userpages.umbc.edu/~neumann/Chem102/Exams2001/Exam01/Image337.gif

Appendix E: Structure of Novolak Resin, DiazoQuinone Sensitizer And DQN complex



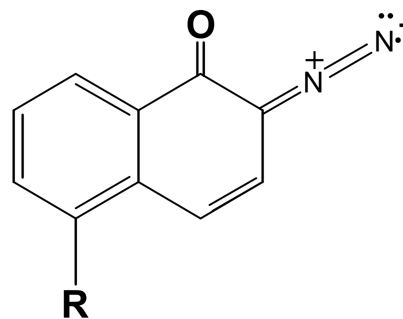


Figure (1)
Meta –Cresol Novolak

Figure (2)
DiazoNaphtoQuinone (DQ)

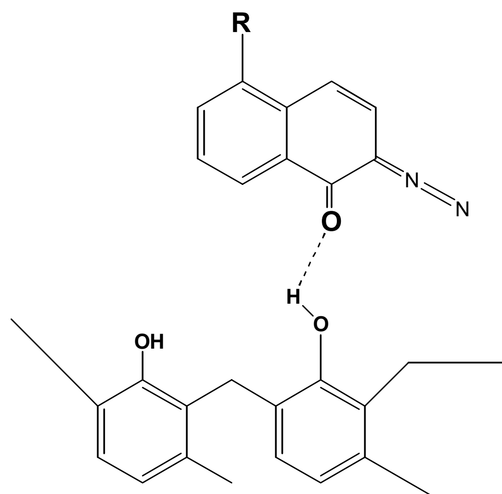
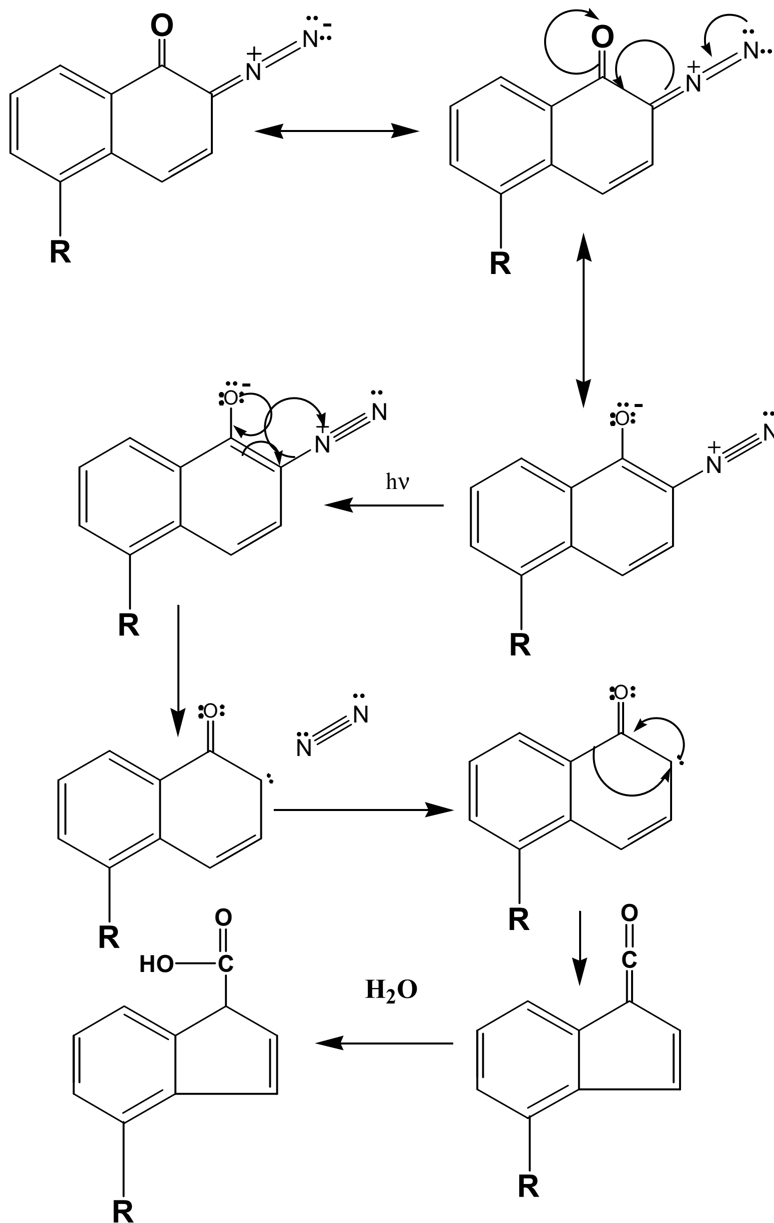


Figure (3)
Novolak- DQ Complex
Moreau 36

Figure 4 Proposed mechanisms for the photoreaction of DiazoQuinone.



Moreau, 1998, p.46)

The mechanism is described by Ueno in Sheats & Smith 1998 p.432 and at http://fachschaft.cup.uni-muenchen.de/~schleifi/reaktion/reaction/wolffuml.html.
I created the above mechanism from the two sources, however both of sources state that there is no agreed upon mechanism for this reaction.

Appendix F: LED Variations

Light Emitting Diode Color Variations

Color Name	Wavelength (Nanometers)	Semiconductor Composition
Infrared	880	GaAlAs/GaAs
Ultra Red	660	GaAlAs/GaAlAs
Super Red	633	AlGaInP
Super Orange	612	AlGaInP
Orange	605	GaAsP/GaP
Yellow	585	GaAsP/GaP
Incandescent White	4500K (CT)	InGaN/SiC
Pale White	6500K (CT)	InGaN/SiC
Cool White	8000K (CT)	InGaN/SiC
Pure Green	555	GaP/GaP
Super Blue	470	GaN/SiC
Blue Violet	430	GaN/SiC
Ultraviolet	395	InGaN/SiC

Table 1
http://www.micro.magnet.fsu.edu/primer/lightandcolor/ledsintro.html

LED Background Information

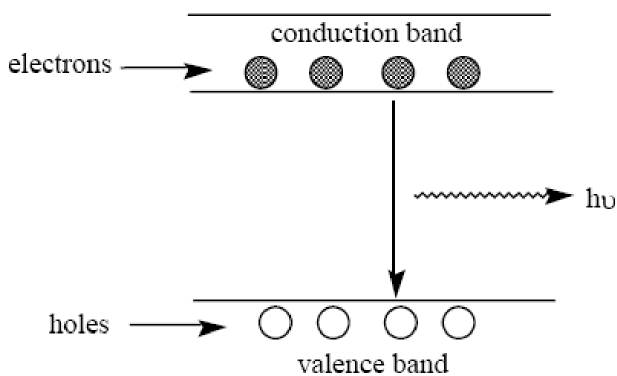


Figure 1: Electron passing from conduction band to the valence band releases energy. If the photon of light has a wavelength in the visible range, "colored" light is observed.

Table 1: Relationship between LED Color, Wavelength and Energy of Light.

Color of Light	Wavelength (nm)	Energy (eV & kJ/mol)
Violet	410	3.0 (290)
Blue	480	2.6 (250)
Green	530	2.3 (225)
Yellow	580	2.1 (205)
Orange	610	2.0 (195)
Red	680	1.8 (175)